ABSTRACT OF THE DISCLOSURE

A defect current contribution elimination technique may be suitable for dynamic random access memories (DRAMs) and other memory devices. A defect current can be eliminated by using an isolation circuit (**106**) between bitlines (**102**-0 and **102**-1) and an associated sense amplifier circuit (**104**). Isolation circuit (**106**) can be controlled by programmable elements, such as fusible links, which are blown at wafer test to isolate the defective bitlines from the sense amplifier circuit. Isolated, defective bitlines may initially float, but based upon the type of defect, such bitlines can be resistively tied to another element, and as a result no DC current will flow. According to another implementation, controllable devices are placed between wordlines (**206**) and the wordline driver circuits (**226**-y). A current path through a defective wordline can be similarly cut-off.